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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,405	08/27/2003	Terry L. Lyon	10971151-3	5330

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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,405	LYON, TERRY L.	
	Examiner	Art Unit	
	Denise Tran	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6* is/are allowed.

6)☒ Claim(s) *7,8 and 10-15* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are presented for examination.

2. The disclosure is objected to because of the following informalities: the current status of the parent application disclosed in page 1 of the current specification should be informed.

Appropriate correction is required.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "receiving first virtual address information in the first TLB" "in parallel . . . receiving the first virtual address information and second virtual address information in the second TLB." Claim 1, line 7; claims 8, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The

replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-12 of U.S. Patent No. 6,625,714. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-12 of the Patent do not direct to a method for

translating. It would have been obvious to one of ordinary skill in the art at the time the invention was made that the method of the current application is performed by the compute architecture as claimed in the Patent. Claims 1-12 of the Patent do not teach small and large sizes of TLBs. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the different sizes of the TLBs because it would allow suitable TLB for particular operations or bandwidth, thereby providing high performance which emphasizes throughput.

6. Claims 7 and 12-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Fu et al., U.S. Patent No. 6,272,597, (hereinafter Fu).

As per claims 7, Fu teaches the invention as claimed, a parallel, distributed function TLB structure(e.g., abstract, and figs.1-2), comprising:

A small TLB having a reduced memory port bandwidth (e.g., fig.1, little TLB0 or TLB1, col. 3, lines 15-24), the small TLB adapted to receive address data consisting of address data associated with integer loads (e.g., fig. 1, VA0 or VA; col. 2, lines 50-55); and

A large TLB having a high memory port bandwidth (e.g., fig. 1, big TLB of a second level L1; col. 4, lines 45-56), the large TLB operable in parallel with the first TLB (e.g., col. 5, lines 10-17; col. 2, line 63 to col. 3, line 5; fig. 3. els 700-710; fig. 4, els. 800-810; fig. 5, els 900-910), the large TLB adapted to receive the address data associated with the integer loads and adapted to receive address data associated with floating point operations and integer store operations (e.g., col. 2, lines 55-57).

As per claim 12, a method to reduce latency and thrashing in a computer architecture having a parallel translation lookaside buffer (TLB) structure (e.g., figs. 1-3, els. 180 and 190; and els. 700 and 710) , the method comprising:

providing integer load address information to a first translation look aside buffer (TLB) using a first bandwidth (e.g., fig. 1, VA0 or VA; col. 2, lines 50-55); and

providing the integer load address information, and other address information, to a second TLB using a second bandwidth larger than the first bandwidth (e.g., fig. 1, big TLB of a second level L1; col. 4, lines 45-56), wherein the integer load address information is provided in parallel to the first and the second TLBs (e.g., col. 5, lines 10-17; col. 2, line 63 to col. 3, line 5; fig. 3. els 700-710; fig. 4, els. 800-810; fig. 5, els 900-910).

As per claim 13, Fu teaches further comprising converting the integer load address information into TLB hit information (e.g., col. 3, lines 15-18 and 57-61) and providing the TLB hit information to a first cache (e.g., fig. 3, el. 730 where a first cache can be cache L1).

As per claim 14, Fu teaches the system further comprising converting the integer load address information, and other address information into physical address information (i.e., physical addresses or hit/miss; e.g., col. 3, lines 15-18 and 57-61; col. 6, lines 15-25); providing the physical address information to a first cache and to a second cache (e.g., col. 3, lines 57-65; col. 4, lines 45-68 and et seq.)

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al., U.S. Patent No. 6,272,597, (hereinafter Fu), as applied to claims 7 and 12 above, and further in view of Naffziger, EP0911737.

As per claim 8, Fu teaches an integer load data cache that receives an output from the small TLB (e.g., fig. 1, el. 230), a data cache that receives an output from the large TLB wherein the large TLB provide physical addresses to the data cache and the data cache hold the physical addresses (e.g., col. 4, line 60 – col. 5, line 5; fig. 1, els 210, 330, 340) but Fu does not explicitly show the small TLB provides TLB hit information based on a virtual address and wherein the integer load data cache stores the TLB hit information. Naffziger shows a TLB provides TLB hit information based on the virtual address (e.g., abstract and fig. 2, els. 212, 214) and wherein the integer load data cache stores (e.g., fig. 2, el. cache section 204, 216 of a cache fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Naffziger into the system of Fu because it would eliminate a time critical path and reducing the cache access time as taught by Naffziger, abstract and col. 5, lines 24-27.

9. Claims 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al., U.S. Patent No. 6,272,597, (hereinafter Fu), as applied to claims 7 and 12, and further in view of Yoshioka et al, U.S. Patent No. 6047354, hereinafter Yoshioka.

As per claims 11 and 15, Fu teaches the second data comprising any data type or storing any type of data in the second TLB (e.g., col. 10, lines 19-20) including integer load (e.g., col. 6, lines 18-20) and cache misses (e.g., col. 5, line 64 to col. 6, line 9). Fu does not explicitly show an exception and privilege information module or receiving/storing exception and privilege information in the second TLB. Yoshioka shows an exception and privilege information module (e.g., fig. 18, els pr check and EX 3-5) and receiving/storing a data for exception and privilege information in a TLB (e.g., fig. 5, els. D and PR and fig.18, els. privilege and exception information). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Yoshioka into the teaching of Fu because it would allow checking the access right and providing memory protection as taught by Yoshioka, col. 13, lines 62-65 and col. 19, lines 7-17.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al., U.S. Patent No. 6,272,597, (hereinafter Fu), as applied to claims 7 and 12 above, and further in view of Beard, Sr. et al, U.S. Patent No. 6351797, hereinafter Beard.

As per claim 10, Fu shows the large TLB and the integer load data cache (e.g., fig. 1, els. 180, 110 or 340). Fu does not explicitly show a store update and invalidate control coupled to the large TLB and the integer load data cache, the store update and invalidate control providing an update or invalidation signal for cache lines in the integer load data cache. Beard shows a store update and invalidate control coupled to the large TLB and the integer load data cache, the store update and invalidate control providing an update or invalidation signal for cache lines in the integer load data cache (e.g., fig. 16, steps 1631, 1621 and col. 29, lines 25-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Beard into the system of Fu because it would allow updating TLBs with the most recently accessed address information and maintaining data coherency, thereby reducing time accessing and increasing speed accessing for the same accessed information in future use.

11. Claims 1-6 are allowable over the prior of record.

12. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and a timely filed terminal disclaimer.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-

9823. The examiner can normally be reached on Monday, Thursday and an alternated Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for central Official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Dennspenn

D.T.
June 24, 2004